

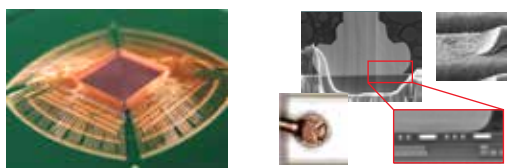
ChipArray® Packages (CABGA/fBGA)

Amkor's ChipArray® Ball Grid Array (CABGA) packages are laminate based packages that are compatible with SMT mounting processes worldwide.

The near chip size CABGA fine-pitch BGA (fBGA) offers a broad selection of ball array pitches (≥ 0.4 mm pitch), ball counts and body sizes (1.5 mm to 27 mm body), single and multi-die layouts, stacked die (1-16) and passive component (up to 300) integration.



Copper (Cu) wire is today's fastest growing interconnect method and Amkor offers high volume infrastructure on latest generation Cu wire bond equipment at all Amkor CABGA production locations.



Thin core laminate (2 to 6 metal layer) from the strongest supply chain in the industry, ultra-thin mold cap thickness and Si thinning below 75 μm enable next generation tablets, mobile handsets, game controllers, digital still & video cameras and remote devices.

Advances in substrate surface finishes and routing techniques reduce gold costs while improving electrical and board level reliability performance. Innovative thermal package structures offer cost competitive solutions to the most challenging thermal management needs.

Applications

The ChipArray package family is applicable for a wide range of semiconductors from high end FPGAs, ASICs to memory, analog, RF devices, MCUs, and simple PLDs requiring a smaller package size than conventional PBGAs or leadframe packages. ChipArray packages fill the need for the low cost, minimum space, high performance and reliability requirements of mobile and gaming devices, notebooks, personal computers, networking, automotive and industrial applications.

Visit [Amkor Technology online](http://www.amkor.com) for locations and to view the most current product information.

CABGA/fBGA

Features

- Cutting edge technology and expanding package offerings provide a platform from prototype-to-production
- Lowest price using Amkor standard CABGA bill of materials selection
- 1.5-27 mm body size available
- Square or rectangle packages available
- 4-700 ball/lead counts
- 0.4, 0.5, 0.65, 0.75, 0.80 & 1.0 mm ball pitch available
- JEDEC MO-216 compliant for 0.8 mm & 1.0 mm ball pitch
- JEDEC MO-195 compliant for 0.5 mm & 0.65 mm ball pitch
- JEDEC MO-298 compliant for 0.4 mm ball pitch
- RoHS-6 (green) BOM options for 100% of CABGA family

Thermal Performance

Body Size (mm)	GJA at 1.0W and 0 Airflow (°C/W)		
	LFBGA	TFBGA	VFBGA
8 x 8	37.28	36.45	37.52
10 x 10	19.86	29.04	26.7
15 x 15	20.1	N/A	N/A
19 x 19	17.04	N/A	N/A

*Additional thermal data available

Reliability Qualification

- Moisture Sensitivity Characterization JEDEC Level 3 @ 260°C; L2 & L1 achievable in some structures/BOMs*
85°C/85% RH, 168 hours
- HAST 130°C/85% RH, 96 hours
- Temp/Humidity 85°C/85% RH, 1000 hours
- Temp Cycle -55°C/+125°C, 1000 cycles
- High Temp Storage 150°C, 1000 hours

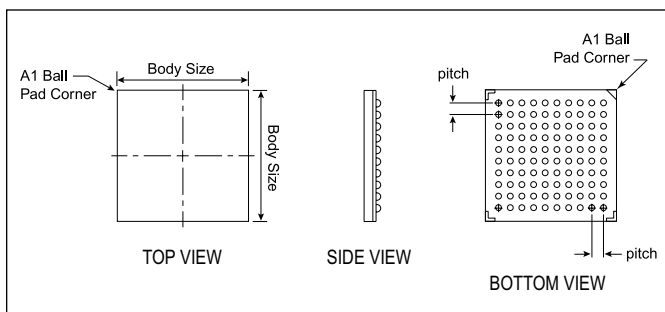
Board level reliability available*

*Contact Amkor for additional information.





CABGA/fBGA



Standard Materials

- Package substrate
 - Conductor: Copper
 - Dielectric: Epoxy resin glass reinforced
- Die attach adhesive: Low stress elastomer
- Encapsulant: Epoxy mold compound
- Low alpha material: Available
- Solder ball: Pb-free
- Wire type: Copper and gold (2N, 4N)

Test Services

- Program generation/conversion
- Product engineering
- Wafer sort
- 256 pin x 20 MHz test system available
- 55°C to +165°C test available
- Burn-in capability
- Tape and reel services

Shipping

- JEDEC trays

Process Highlights

- Die thickness: 0.075-0.27 mm
- Marking: Laser
- Ball inspection: Optical
- Pack options: Dry pack
- Wafer backgrinding: Available
- Encapsulated SMT components: Available
- Micro Pb-free covered LGA Pads/LGAs: Available

CABGA Package Thickness Capability

	LFBGA > 1.2 mm	TFBGA 1.2 mm (max)	VFBGA 1.0 mm (max)	WFBGA 0.8 mm (max)	UFBGA 0.65 mm (max)	XFBGA 0.50 mm (max)
	CA-1fBGA	CABGA-tfBGA CTBGA/CASON	CABGA-vfBGA CVBGA/CASON	CA-wfLGA CASON	CA-ufLGA	CA-xfLGA
Mold Cap Thickness	0.70 mm 0.95 mm	0.60 mm 0.53 mm	0.45 mm (BGA) 0.53 mm (LGA)	0.40 mm (BGA) 0.45 mm (LGA)	0.32 mm (BGA)* 0.40 mm (LGA)	0.25 mm (BGA) 0.32 mm (LGA)
Substrate Layer	2lyr 0.32 mm, 0.56 mm 4lyr or 6lyr 0.34 mm, 0.56 mm	2lyr or 4lyr 0.21 mm, 0.26 mm	2lyr or 4lyr 0.21 mm	2lyr 0.21 mm, 0.13 mm	2lyr 0.13 mm	2lyr 0.13 mm
Die Thickness**	0.27 mm	0.23 mm	0.18 mm	0.13 mm	0.10 mm	0.075 mm
Availability	0.7 mm All Sites 0.95 mm P3, K4	All Sites	All Sites	0.45 mm All Sites 0.40 mm C3, K4	0.32 mm (K4 only)	0.25 mm All Sites

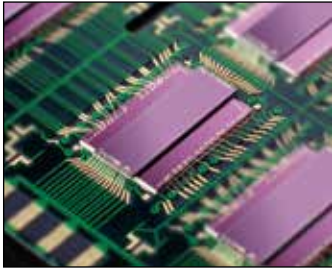
*Options are available with microballs.

**Die thickness is also dependent on the wirebond loop height requirement.

Visit Amkor Technology online for locations and to view the most current product information.



With respect to the information in this document, Amkor makes no guarantee or warranty of its accuracy or that the use of such information will not infringe upon the intellectual rights of third parties. Amkor shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon it and no patent or other license is implied hereby. This document does not in any way extend or modify Amkor's warranty on any product beyond that set forth in its standard terms and conditions of sale. Amkor reserves the right to make changes in its product and specifications at any time and without notice. © 2013, Amkor Technology Incorporated. All Rights Reserved.



Stacked CSP (SCSP)

The Stacked CSP (SCSP) family leverages Amkor's industry-leading ChipArray® Ball Grid Array (CABGA) manufacturing capabilities. This broad, high-volume infrastructure enables the rapid deployment of advances in die stacking technology across multiple products and factories to achieve lowest total cost requirements.

Stacked CSP technology enables the stacking of a wide range of different semiconductor devices to deliver the high level of silicon integration and area efficiency required in portable multi-media products.

Stacked CSP utilizes high density thin core substrates, advanced materials (ie: thin film die attach adhesive, fine filler epoxy mold compound), along with leading-edge wafer thinning, die attach, wire bonding and molding capabilities to stack multiple devices in a conventional fine pitch BGA (FBGA) surface mount component. These advanced assembly capabilities in combination with Amkor's expertise in design and test, enable stacks up to 16 active devices while optimizing yield and mounted height requirements.

Many customers have relied on Amkor to solve their highest density and most complex device stack combinations. As a result, Amkor has established industry leadership in stacking pure memory, mixed signal, and logic + memory devices, including NAND, NOR and DRAM memory, digital base band or applications processors + high density flash or mobile DRAM devices. Designers are looking to Stacked CSP technologies to achieve a high level of integration, along with size and cost reductions in future chip set combinations.



Visit Amkor Technology online for locations and to view the most current product information.

www.amkor.com

Stacked CSP

Applications

Portable multi-media devices including cell phones, digital cameras, PDAs, audio players and mobile gaming employ SCSP solutions to address a range of design requirements, including:

- Higher memory capacity and more efficient memory architectures
- Smaller, lighter and more innovative product form factors
- Lower cost and more space efficient

Features

- 4-21 mm body size
- Package height down to 0.6 mm
- High die count pure memory, eMMC and All in One stacks
- Design, assembly and test capabilities that enable stacking of DRAM with Logic or Flash memory devices
- Logic/Flash, digital/analog and other ASIC/memory combinations of 320 I/O and greater
- Established package infrastructure with standard CABGA footprints
- Consistent product performance, high yields and reliability
- JEDEC standard outlines including MO-192 and MO-219
- Thin DA film and spacer technology
- Extended die overhang wire bonding
- Low loop wire bonding less than 45 µm
- Vacuum transfer and compression molding
- Wafer thinning/handling to 30 µm
- Pb free, RoHS compliant and green materials
- Passive component integration options

Reliability Qualification

Amkor assures reliable performance by continuously monitoring key indices, including:

Package Level:

- | | |
|---|---------------------------------------|
| • Moisture Sensitivity Characterization | JEDEC Level 3 @ 260°C; |
| • Additional Test Data at | [(30°C/85% RH, 96 hours)+260] x2 or 3 |
| • HAST | 130°C/85% RH, 96 hours |
| • Temp/Humidity | 85°C/85% RH, 1000 hours |
| • Temp Cycle | -55°C/+125°C, 1000 cycles |
| • High Temp Storage | 150°C, 1000 hours |

Board Level:

- | | |
|-----------------|---------------------------|
| • Thermal Cycle | -40°C/+125°C, 1000 cycles |
|-----------------|---------------------------|



Stacked CSP

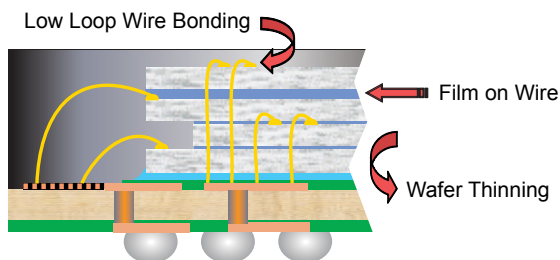
Process Highlights

- Die qty, stack Up to 16 high die configurations
- Ball pad pitch 0.3, 0.4, 0.5, 0.65, 0.75, 0.8 mm
- Die thickness (min) Down to 30 μm
- Laminate core thickness 40, 50, 60, 100 or 150 μm
- Ball diameter 0.25, 0.30, 0.40, 0.46 mm
- Die bond pitch (min) 40 μm (In-line) with roadmap to 25 μm
- Wirebond length (max) 5 mm (200 mils)
- Wirebond dia (min) 15, 18, 20, 25, 30 μm
- Low loop wirebonding 45 μm
- Wafer thinning 200 & 300 mm wafers

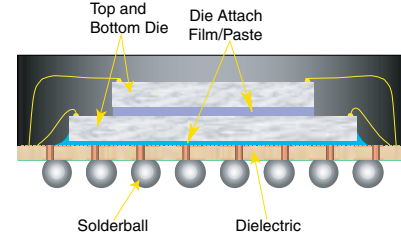
Standard Materials

- Package substrate
 - Dielectric Laminate (e.g., DS7409, E679, BT)
 - Layer count (laminate) Polyimide (e.g., Kapton®) 2-4
- Die attach Film DA compatible with all passivation types
- Wire type Gold, Cu, PCC High tensile strength
- Encapsulant Thixotropic epoxy (black)
- Solder balls 63Sn/37Pb & PbFree Sn/3-4Ag/0.5Cu
- Device type Silicon, SiGe, etc.
- Marking Laser

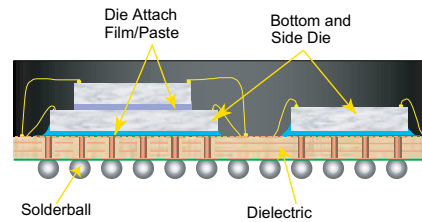
Stacked CSP Key Technologies



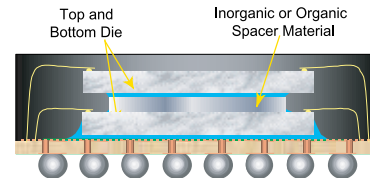
Stacked CSP Cross Section 2 Die on 2-Layer Laminate Structure



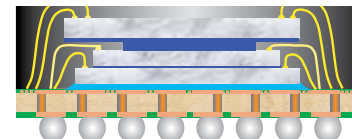
Stacked CSP Cross Section 2 + 1 Die on 4-Layer Laminate Structure



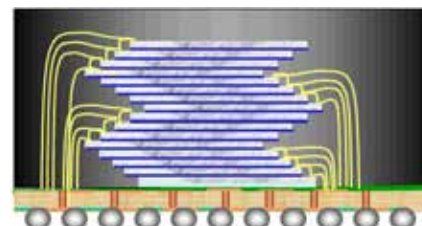
Same Size (SS) Die Stacked CSP Cross Section 2 Die on 2-Layer Laminate Structure



Stacked CSP Cross Section 3 + 1 Logic + Memory



Stacked CSP Cross Section 16 + 0 Die Memory



Visit Amkor Technology online for locations and to view the most current product information.



With respect to the information in this document, Amkor makes no guarantee or warranty of its accuracy or that the use of such information will not infringe upon the intellectual rights of third parties. Amkor shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon it and no patent or other license is implied hereby. This document does not in any way extend or modify Amkor's warranty on any product beyond that set forth in its standard terms and conditions of sale. Amkor reserves the right to make changes in its product and specifications at any time and without notice. © 2013, Amkor Technology Incorporated. All Rights Reserved.

DS573J
Rev Date: 4/13



Flip Chip CSP Packages (fcCSP)

Amkor Technology offers the Flip Chip CSP (fcCSP) package – a flip chip solution in a CSP package format. This package construction utilizes Pb-Free (or Eut. SnPb) flip chip interconnect technology, in either area array or peripheral bump layout, replacing standard wirebond interconnect. The advantages of flip chip interconnect are multiple: it provides enhanced electrical performance over standard wirebond technology, it allows for a smaller form factor due to increased routing density, and the elimination of wire-bond loops. Current wafer bump technology and flip chip assembly process allows for peripheral flip chip bumping or area array bumping, with either solder or Cu pillar bump technology.

The fcCSP is based on Amkor's proprietary ChipArray® BGA (CABGA) package construction, using cutting edge thin core laminate substrates. The package is assembled in strip format, in either bare die or overmolded format, and saw singulated for manufacturing efficiency and cost minimization. Pattern plating for fine line/spaces, via-in-pad substrate structure, and thin core substrate panel processing allow for increased routing density and enhanced electrical performance, making fcCSP an attractive option for advanced CSP applications where electrical performance is a critical factor.

The fcCSP is available in both thin core laminate substrate technology as well as build up (for further enhanced routing). Package size ranges from 2 mm to 17 mm, accommodating BGA ball pitches from 0.4 mm to 1.0 mm. In addition to BGA technology, the fcCSP is also available in LGA format, allowing for a lower minimum package thickness.

Features

- Can design to high frequency applications of 60+ GHz
- 9-1500+ ball counts
- Target market – cell phones, handheld electronics, applications where high density packaging is required, multi-die and/or designs with passive components
- Array strip production
- Thin core laminate or buildup substrate construction
- Bare die with underfill, overmolded, molded underfill and exposed die molded versions available
- Accommodates package sizes from 2 mm to 17 mm
- Flip chip bump pitches of 80 μm peripheral and 130 μm area array

fcCSP

- Cu pillar flip chip interconnect for fine bond pitches down to 30 μm/60 μm staggered
- Available in 0.4-1.0 mm BGA ball pitch, as well as LGA interconnect
- Minimum package thickness of < 0.4 mm for LGA interconnect, < 0.6 mm for 0.4 mm and 0.5 mm BGA pitch
- Turnkey Solution – design, bumping, bumped wafer probe, backgrind, assembly, test
- Much better signal to noise ratio at higher frequencies (>1 GHz) versus wirebonded packages
- Low inductance of flip chip bumps – short, direct signal path
- Flexible customizable substrate routing. Smaller possible body size than wirebond CSP due to additional space not required for wirebond pads

Applications

The fcCSP package is an attractive option for handheld/portable electronics where, in addition to performance, package size is critical. Some applications which have adopted fcCSP are high-performance workstations, servers, data communication products and some emerging applications such as netbooks and RF applications where electrical performance is critical. The elimination of wirebond loops allows for a low inductance connection to the die while the increased routing density enables optimized electrical paths for critical high frequency signal lines.

Thermal Performance

Theta JA (°C/W)

- 12 x 12 mm, 441 lead package with 7.5 mm x 7.5 mm die, 0.5 mm pitch, 0.45 mm mold cap
- 0 LFPM, 4 layer PC board
- Junction ambient thermal resistance = 21.3°C/W

Electrical Performance

8 x 8 mm body, 176 lead, 0.5 mm ball pitch, simulated results @ at 100 MHz

	Min	Max
Inductance	0.34 nH	2.15 nH
Capacitance	0.19 pF	0.64 pF
Resistance	22 mΩ	84 mΩ

Reliability Qualification

Package Level:

- Laminate Moisture Sensitivity JEDEC Level 3 @ 260°C 30°C/60% RH, 192 hours
- Ceramic Moisture Sensitivity JEDEC Level 1 @ 260°C 85°C/85% RH, 168 hours
- PCT 121°C/100% RH, 96 hours
- Temp/Humidity 85°C/85% RH, 1000 hours
- Temp Cycle -55°C/+125°C, 1000 cycles
- High Temp Storage 150°C, 1000 hours

Board Level:

8 mm body, 64 lead, 0.33 mm PWB NSMD pad size

- Thermal Cycle -40°C/+125°C, 1 cycle/hour, 3000 cycles
- Thermal Cycle -40°C/+125°C, 2 cycles/hour, 2500 cycles

17 mm body, 1019 lead

- Thermal Cycle 0°C/+100°C, 1 cycle/hour, 2230 cycles

Visit Amkor Technology online for locations and to view the most current product information.

fcCSP

Process Highlights

- Die size: 0.5 mm to 13 mm
- Package size: 2 mm to 17 mm
- Bump pitch (LF or Eutectic)
 - In-line: 80 μm
 - Array: 130 μm
- Bump pitch (Cu pillar)
 - In-line: 30/60 μm staggered
 - Array: 130 μm

Standard Materials

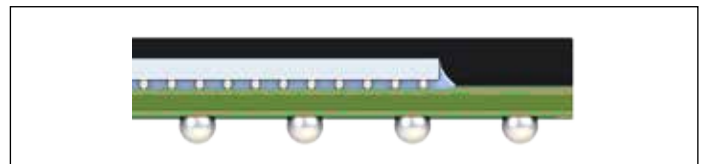
- Package substrate:
 - NXA, NS, NS-LC, NSF-LCA
 - E679: FG, FGB, FGBS, GT
 - E700G, E705G
 - DS7409HG, DS7409HGB(S), DS7409HGB(LE)
 - ELC4785GSB, ELC4785THB, ELC4785THG
- Bump: Pb-Free, Eutectic, Cu pillar
- Encapsulant: Epoxy mold compound
- Solder balls: Lead free, Eutectic, Pb-Free

Test Services

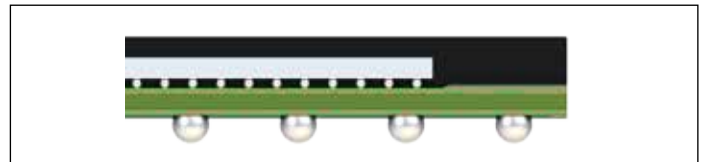
- Program generation/conversion
- Product engineering
- Wafer sort
- -55°C to +165°C test available
- Burn-in capabilities
- Tape and reel services

Shipping

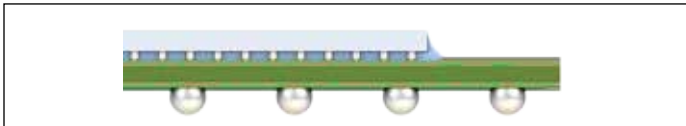
- JEDEC trays



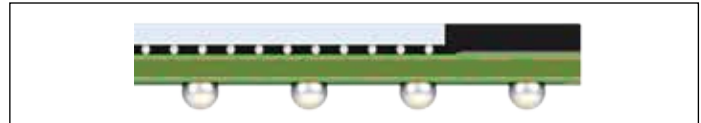
Overmolded,
Capillary Underfill



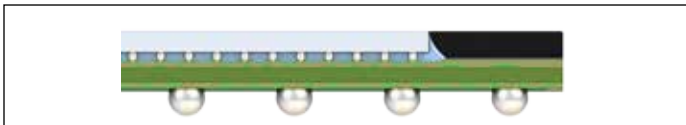
Overmolded,
Molded Underfill



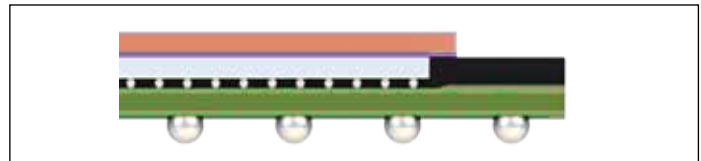
Bare Die,
Capillary Underfill



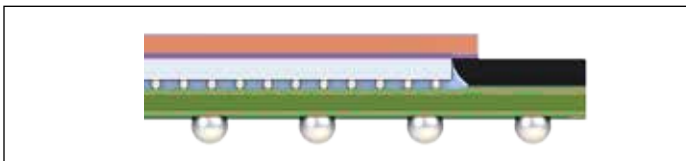
Exposed Die,
Molded Underfill



Exposed Die Molded,
Capillary Underfill



Exposed Die Molded,
Molded Underfill
Plate Heatsink



Exposed Die Molded,
Capillary Underfill
Plate Heatsink

Visit Amkor Technology online for locations and to view the most current product information.

fcCSP

Configuration Options

fcCSP Package Dimensions (mm)

Pkg X	Pkg Y	# BGAs	Ball Dia.	BGA Pitch
06.5	08.5	52	0.300	0.50
06.0	05.0	102	0.250	0.45
06.0	06.0	90	0.300	0.50
06.0	06.0	137	0.200	0.40
06.5	06.5	97	0.250	0.40
06.5	06.5	225	0.250	0.40
06.5	06.5	225	0.250	0.40
07.0	07.0	64	0.450	0.80
07.0	07.0	88	0.300	0.50
07.0	07.0	88	0.300	0.50
07.0	07.0	132	0.300	0.50
07.0	07.0	191	0.250	0.40
07.0	07.0	208	0.250	0.40
07.0	07.0	287	0.250	0.40
07.0	07.0	287	0.250	0.40
09.0	09.0	192	0.300	0.50
09.0	09.0	196	0.300	0.50
09.0	09.0	383	0.250	0.40
09.0	09.0	383	0.250	0.40
09.0	09.0	383	0.250	0.40
09.5	09.0	330	0.250	0.40
09.5	09.0	330	0.200	0.40
10.0	10.0	144	0.460	0.80
10.0	10.0	144	0.400	0.80
10.0	10.0	108	0.400	0.80
10.0	10.0	249	0.250	0.525/0.67
10.0	10.0	249	0.250	0.53
10.0	10.0	384	0.250	0.40
10.0	10.0	424	0.250	0.40
10.0	10.0	454	0.250	0.40
11.0	08.0	300	0.250	0.40
11.0	11.0	301	0.300	0.50
11.0	11.0	456	0.250	0.40
11.0	11.0	576	0.250	0.40
11.0	11.0	576	0.250	0.40
11.0	11.0	576	0.250	0.40
12.0	12.0	121	0.600	1.00
12.0	12.0	168	0.250	0.50
12.0	12.0	216	0.250	0.40
12.0	12.0	216	0.250	0.40
12.0	12.0	409	0.250	0.40
12.0	12.0	441	0.300	0.50
12.0	12.0	441	0.300	0.50

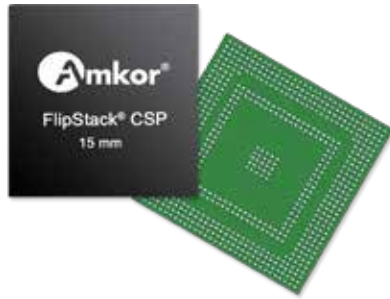
Pkg X	Pkg Y	# BGAs	Ball Dia.	BGA Pitch
12.0	12.0	512	0.250	0.40
12.0	12.0	512	0.250	0.40
12.0	12.0	515	0.250	0.50
12.0	12.0	524	0.250	0.40
12.0	12.0	547	0.250	0.40
12.0	12.0	547	0.250	0.40
12.0	12.0	560	0.250	0.40
12.0	12.0	560	0.250	0.40
12.0	12.0	560	0.250	0.40
12.0	12.0	560	0.250	0.40
12.0	12.0	569	0.250	0.40
12.0	12.0	580	0.250	0.40
12.0	12.0	617	0.250	0.40
12.0	12.0	617	0.200	0.40
12.0	12.0	697	0.250	0.40
12.0	12.0	700	0.200	0.40
12.0	12.0	714	0.250	0.40
13.0	13.0	225	0.460	0.80
14.0	14.0	220	0.325	0.50
14.0	14.0	240	0.250	0.50
14.0	14.0	240	0.225	0.50
14.0	14.0	240	0.225	0.50
14.0	14.0	256	0.250	0.40
14.0	14.0	256	0.250	0.40
14.0	14.0	256	0.250	0.40
14.0	14.0	256	0.250	0.40
14.0	14.0	256	0.250	0.40
14.0	14.0	289	0.460	0.80
14.0	14.0	289	0.460	0.80
14.0	14.0	617	0.300	0.50
14.0	14.0	676	0.250	0.50
14.0	14.0	681	0.250	0.5/0.707
14.0	14.0	756	0.250	0.40
14.0	14.0	789	0.250	0.40
14.0	14.0	976	0.250	0.40
14.0	14.0	976	0.200	0.40
14.0	14.0	980	0.250	0.40
15.0	15.0	216	0.325	0.50
15.0	15.0	216	0.300	0.50
15.0	15.0	249	0.300	0.80
15.0	15.0	324	0.500	0.80
15.0	15.0	841	0.200	0.50

Visit Amkor Technology online for locations and to view the most current product information.



With respect to the information in this document, Amkor makes no guarantee or warranty of its accuracy or that the use of such information will not infringe upon the intellectual rights of third parties. Amkor shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon it and no patent or other license is implied hereby. This document does not in any way extend or modify Amkor's warranty on any product beyond that set forth in its standard terms and conditions of sale. Amkor reserves the right to make changes in its product and specifications at any time and without notice. © 2013, Amkor Technology Incorporated. All Rights Reserved.

DS577G
Rev Date: 10/13



FlipStack® CSP

The FlipStack CSP family utilizes Amkor's industry leading ChipArray® Ball Grid Array (CABGA) manufacturing capabilities, in combination with Amkor's fcCSP technology. This broad high volume infrastructure enables the rapid deployment of advances in die stacking technology across multiple products and factories to achieve lowest total cost.

FlipStack CSP technology enables the stacking of a wide range of different semiconductor devices to deliver the high level of silicon integration and area efficiency required in portable multi-media products. This type of packaging uses high density thin core substrates, advanced wafer thinning, die attach, flip chip and wire bonding capabilities to stack multiple devices in a conventional fine pitch BGA (FBGA) surface mount package. Many customers have relied on Amkor to solve their highest density and most complex device stack combinations. As a result, Amkor has established industry leadership in stacking complex mixed signal, logic + memory devices, including digital base band or application/processors + high density flash or mobile DRAM devices. Designers are looking to FlipStack CSP technologies to achieve integration, size and cost reductions in chip set combinations.

Applications

FlipStack CSP technology enables smaller, lighter and more innovative new product form factors at a lower cost. This solution addresses a range of design requirements, and enables a wide variety of applications, including: portable multi-media devices (cell phones, digital cameras, PDAs and audio players).

FlipStack® CSP

Features

- 4-15 mm body size
- Package height down to 0.6 mm
- Design, assembly and test capabilities that enable stacking combinations of memory, logic and mixed signal type devices in I/O counts from 50 to 1100
- Established package infrastructure with standard CABGA and fcCSP footprints
- Consistent product performance with high yields and reliability
- Die overhang wire bonding
- Low loop wire bonding to 40 μm or less.
- Wafer thinning: wire bond to 40 μm , bumped wafer to 75 μm , cu pillar bumped wafer to 50 μm
- Pb free, RoHS compliant and green materials
- Passive component integration options
- JEDEC standard outlines including MO-192, MO-195, MO-216, MO-219 and MO-298

Reliability Qualification

Amkor assures reliable performance by continuously monitoring key indices:

- | | |
|-------------------------------|---------------------------------|
| • Moisture Resistance Testing | JEDEC Level 3 @ 260°C |
| • Unbiased Autoclave/PCT | 121°C/100% RH, 2 atm, 168 hours |
| • Temp/Humidity | 85°C/85%RH, 1000 hours |
| • Temp Cycle | -55°C/+125°C, 1000 cycles |
| • High Temp Storage | 150°C, 1000 hours |

Board Level:

- | | |
|-----------------|---------------------------|
| • Thermal Cycle | -40°C/+125°C, 1000 cycles |
|-----------------|---------------------------|

Visit Amkor Technology online for locations and to view the most current product information.

FlipStack® CSP

Process Highlights

- Ball pad pitch 0.4, 0.5, 0.65, 0.75, 0.8, 1.0 mm
- Die thickness (flip chip) As thin as 70 μm
- Die thickness (wirebond) As thin as 50 μm
- Laminate core thickness 60, 100 or 150 μm
- Ball diameter 0.18, 0.20, 0.22, 0.25, 0.3, 0.4, 0.46 mm
- Wirebond pitch (min) 40 μm in-line with road map to 25 μm
- Bump pitch mass reflow 80 μm In-line, 130 μm array
- Thermal compression: 30 μm /60 μm staggered peripheral 150 μm array
- Wirebond length (max) 5 mm (200 mils)
- Wirebond dia (min) 0.7, 0.8, 0.9, 1.0 mil+ in gold, silver or copper wire bond diameters
- Wafer thinning 150, 200 & 300 mm wafers

Standard Materials

- Package substrate
 - Laminate dielectric
 - HL832: NXA, NS, NS-LC, NSF-LCA
 - E679: FG, FGB, FGBS, GT
 - E700G, E705G
 - DS7409HG, DS7409HGB(S), DS7409HGB(LE), ELC4785GSB, ELC4785THB, ELC4785THG
 - Layer count (laminate) 2-6
- Die attach
 - Bottom die Flip chip attached by mass reflow or thermal compression
 - Top die Non-conductive epoxy, film
- Wire type Au, Cu or Ag
- Encapsulant Transfer molded epoxy
- Underfill Dispensed
- Bumps (F/C die) Pb-free, Eutectic, Cu Pillar
- Solder balls Eutectic, Pb-free
- Device type Silicon, SiGe, GaAs, Glass (IPD film on glass)
- Marking Laser

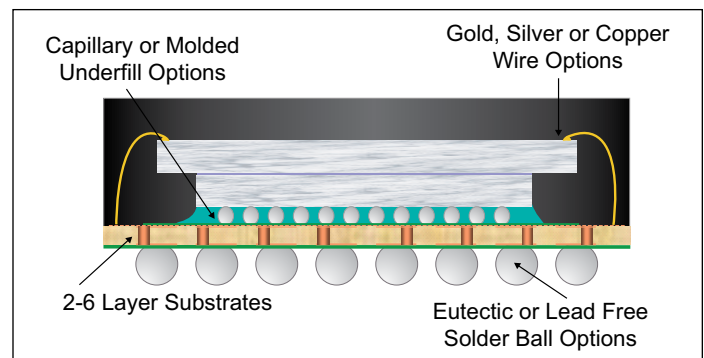
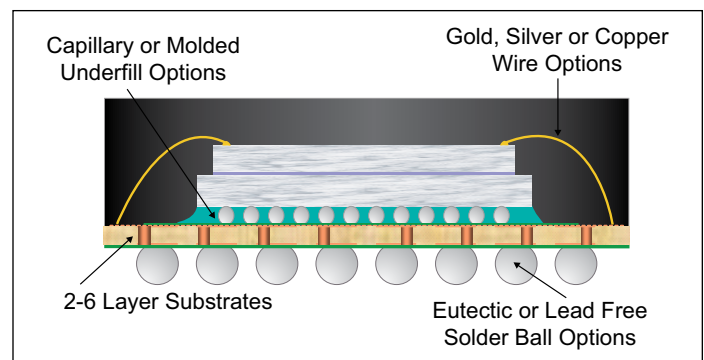
Test Services

- Program generation/conversion
- Product engineering
- Wafer sort
- -55°C to +165°C test available
- Burn-in capabilities
- Tape and reel services

Shipping

- JEDEC trays

Cross-section FlipStack® CSP



Wide range of die size combinations supported.

Contact Amkor for the latest FlipStack® packaging capabilities.

Visit [Amkor Technology online](http://www.amkor.com) for locations and to view the most current product information.



With respect to the information in this document, Amkor makes no guarantee or warranty of its accuracy or that the use of such information will not infringe upon the intellectual rights of third parties. Amkor shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon it and no patent or other license is implied hereby. This document does not in any way extend or modify Amkor's warranty on any product beyond that set forth in its standard terms and conditions of sale. Amkor reserves the right to make changes in its product and specifications at any time and without notice. © 2013, Amkor Technology Incorporated. All Rights Reserved.