

Flip Chip BGA Packages (fcBGA)

Flip chip interconnect utilizes array interconnect of die to substrate as a replacement for conventional wire bonding. This allows the entire die surface to be used for electrical connections to the substrate, exponentially increasing the I/O per unit area vs. perimeter interconnect technologies. Using flip chip interconnect improves package electrical performance by removing the high inductance wires and replacing them with low inductance solder connections. Flip chip interconnect also allows highly parallel, direct connection with on-die power planes, which enables performance at lower operating voltages.

Amkor fcBGA packages are assembled around state-of-the-art, single unit laminate or ceramic substrates. Utilizing multiple high density routing layers, laser drilled blind, buried, and stacked vias, and ultra fine line/space metallization, fcBGA substrates have the highest routing density available. By combining flip chip interconnect with ultra advanced substrate technology, fcBGA packages can be electrically tuned for maximum electrical performance. Once the electrical function is defined, the design flexibility enabled by flip chip also allows for significant options in final package design. Amkor offers fcBGA packaging in a variety of product formats to fit a wide range of end application requirements.

Applications

This IC packaging technology is applicable for high pincount and/or high performance ASICs. Large body fcBGAs provide package solutions for the demands of internet, workstation processors and high bandwidth system communication devices. By incorporating flip chip interconnect technology, packages supporting thousands of connections are enabled in conventional surface mount package sizes. fcBGAs are also the package of choice for gaming system processors and graphics, as well as high-end applications processors for leading-edge portable devices.

Visit [Amkor Technology online](http://www.amkor.com) for locations and to view the most current product information.

www.amkor.com

fcBGA

Features

- Die sizes up to 26 mm
- Package sizes from 10 mm to 55 mm (60 mm and 65 mm in development)
- 0.4 mm, 0.5 mm, 0.65 mm, 0.8 mm and 1.0 mm pitch BGA footprints
- 130 μ m minimum array bump pitch
- < 100 μ m minimum peripheral bump pitch

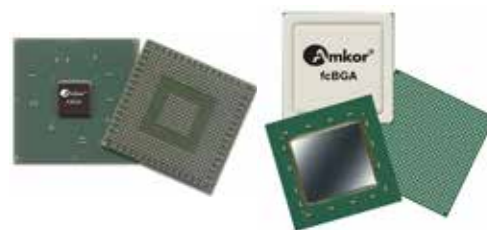
Technology Options

- Substrates
 - 4-16 layer laminate build up substrates
 - High CTE ceramic
 - LTCC alumina ceramic
 - Coreless
- Bump Types
 - Eutectic Sn/Pb
 - High Pb
 - Pb Free
 - Cu pillar (array and fine pitch peripheral)
- Package Formats
 - Bare die
 - Overmolded (FC^MBGA)
 - Lidded

Thermal Solutions

The variety of fcBGA package options allows package selection to be tailored to the specific thermal needs of the end product. High performance ASIC products typically utilize a lidded format that features a controlled bondline die attach direct to a copper heat spreader. This feature produces the lowest possible thermal resistance (Theta JC) between the package and any externally applied thermal solution. The copper heat spreader effectively spreads heat laterally away from the die to the package perimeter and into the motherboard.

Lower wattage products generally utilize bare die or molded configurations. In these cases, the flip chip construction, with solder bumps and core vias, provides a lower resistance path from the active side of the die through the substrate, allowing heat dissipation both from the package surface and into the motherboard.



fcBGA

Additional Package Options

- Wafer Node ≥ 28 nm qualified, 20 nm in development
- SMT components on top or bottom side
- Multi-die capability
- Memory components on top side
- Variety of lid material options
- Grounded lid
- Custom BGA footprints

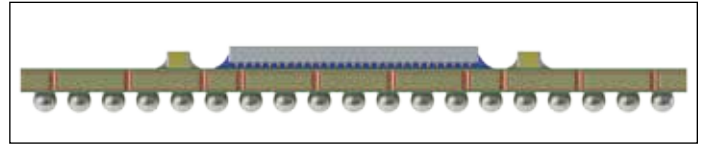
Test Services

- Program generation/conversion
- Product engineering
- Available test/handling technology
- Burn-in capabilities

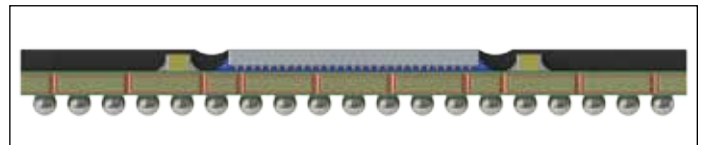
Shipping

- Standard JEDEC trays

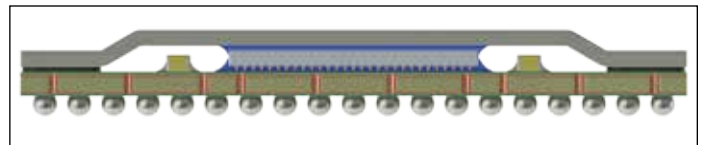
Cross-section fcBGA



Bare Die fcBGA



FCMBGA



Lidded fcBGA

Configuration Options

Full Array Ball Counts (Ball Count Shown Indicates Maximum Package Size Produced to Date)

| Body Size | 0.4 mm | 0.5 mm | 0.65 mm | 0.8 mm | 1 mm |
|-----------|------------|------------|------------|------------|------------|
| | Ball Count | Ball Count | Ball Count | Ball Count | Ball Count |
| 10 | 576 | 361 | 196 | 121 | 81 |
| 11 | 676 | 441 | 256 | 144 | 100 |
| 12 | 841 | 529 | 289 | 196 | 121 |
| 13 | 961 | 625 | 361 | 225 | 144 |
| 14 | 1156 | 729 | 400 | 256 | 169 |
| 15 | 1296 | 841 | 484 | 289 | 196 |
| 16 | 1521 | 961 | 529 | 361 | 225 |
| 17 | | | 625 | 400 | 256 |
| 19 | | | 784 | 484 | 324 |
| 21 | | | 961 | 625 | 400 |
| 23 | | | 1156 | 729 | 484 |
| 25 | | | 1369 | 900 | 576 |
| 27 | | | | 1024 | 676 |
| 29 | | | | 1225 | 784 |

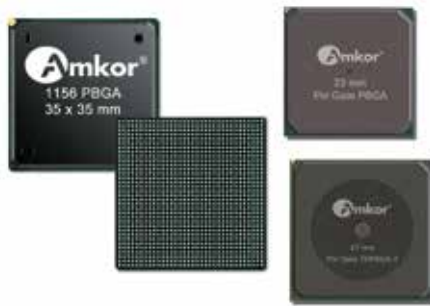
| Body Size | 0.4 mm | 0.5 mm | 0.65 mm | 0.8 mm | 1 mm |
|-----------|------------|------------|------------|------------|------------|
| | Ball Count | Ball Count | Ball Count | Ball Count | Ball Count |
| 31 | | | | 1369 | 900 |
| 33 | | | | 1600 | 1024 |
| 35 | | | | 1764 | 1156 |
| 37.5 | | | | 2025 | 1296 |
| 40 | | | | | 1521 |
| 42.5 | | | | | 1681 |
| 45 | | | | | 1936 |
| 47.5 | | | | | 2116 |
| 50 | | | | | 2401 |
| 52.5 | | | | | 2601 |
| 55 | | | | | 2916 |
| 57.5 | | | | | 3136 |
| 60 | | | | | 3481 |
| 65 | | | | | 4096 |

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DS831B
Rev Date: 10/13



Plastic Ball Grid Array (PBGA)

Amkor's PBGA packages incorporate the most advanced assembly processes and designs for cost/performance applications. This advanced IC package technology allows application and design engineers to optimize innovations while maximizing the performance characteristics of semiconductors.

These PBGA packages are designed for low inductance, improved thermal operation and enhanced SMT ability. Custom performance enhancements, like ground and power planes, are available for significant improvements in electrical response demanded by advanced electronics.

Additionally, these packages utilize industry proven, semiconductor grade materials for reliable, long-term operations while providing user flexible design parameters.

Applications

The integrated design features of Amkor's PBGAs offer enhanced performance in many devices, making this the ideal package for: microprocessors, microcontrollers, ASICs, gate arrays, memory, DSPs, PLDs, graphics and PC chip sets.

Applications requiring improved portability, form-factor/size and high-performance such as cellular, wireless telecommunications, PCMCIA cards, Global Positioning Systems (GPS), laptop PCs, netbooks, video cameras, disc drives and similar products benefit from Amkor's PBGA attributes.

PBGA

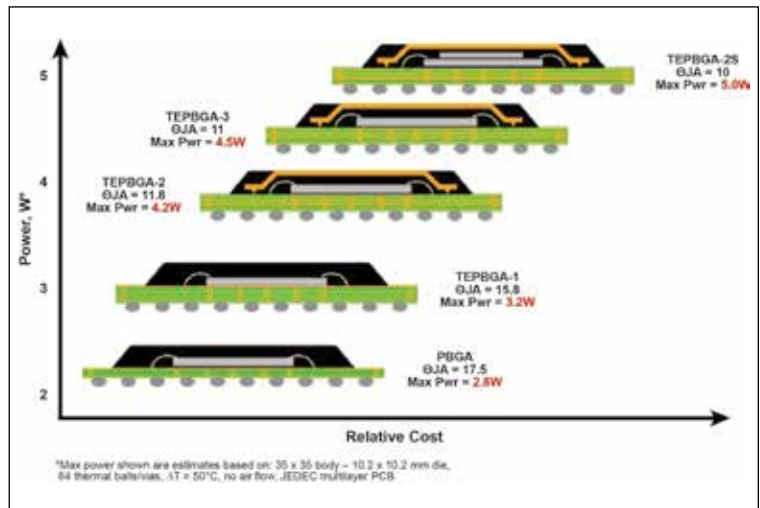
Features

Innovative designs and expanding package offerings provide a platform from prototype-to-production.

- Custom ball counts up to 1521
- 1.00, 1.27 & 1.50 mm standard ball pitch available (other ball pitches available upon request, (e.g. 0.8 mm))
- 17 mm to 40 mm body sizes
- Thin Au wire (0.5 mil) or Cu wire compatible
- Chip-on-Chip (CoC)
- Large mold cap for quality enhancement
- Low profile and lightweight
- Thermal and electrical enhancement capable
- Highly flexible internal routing of signal, power and ground for device performance and system compatibility
- HDI designs possible
- Suitable substrate for multi-die (MCM) and integrated SMT structures
- Mature strip based manufacturing process with high yields
- Full in-house design capability
- Quickest design-to-prototype delivery
- Perimeter, stagger and full ball arrays
- Special packaging for memory available
- Multi-layer, ground/power
- JEDEC MS-034 standard outlines
- Excellent reliability
- 63 Sn/37 Pb Eutectic or Pb-free solder balls

Thermal Performance

Thermal Performance vs. Cost



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DS520Q
Rev Date: 11-14

PBGA

Reliability Qualification

Amkor assures reliable performance by continuously monitoring key indices:

- Moisture Sensitivity Characterization JEDEC Level 3, 30°C/60% RH, 192 hours
- uHAST 130°C/85% RH, 96 hours
- Temp Cycle -55°C/+125°C, 1000 cycles
- High Temp Storage 150°C, 1000 hours

Process Highlights

- Die thickness 13 mils
- Bond pad pitch (min) 2.4 mils
- Au wire diameter 1.2-0.5 mils
- Cu wire diameter 1.2-0.7 mils
- Marking Laser
- Ball inspection Optical
- Pack/ship options JEDEC trays, dry pack
- Wafer backgrinding Available

Standard Materials

- Package substrate CCL-HL832HX-A
- Die attach adhesive Ablestik 2300
- Wire Au HTS/Cu PCC
- Mold compound Nitto GE100L/Sumitomo G770FE
- Solder balls Leaded or lead-free options

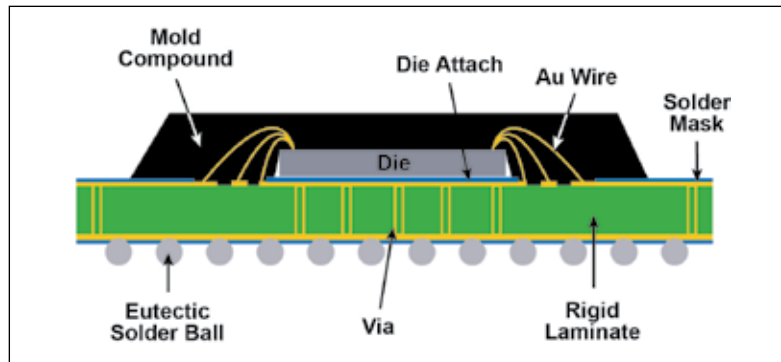
Test Services

- Program generation/conversion
- Product engineering
- Wafer sort
- 256 pin x 20 MHz test system available
- 55°C to +125°C test available
- Burn-in capabilities
- Tape and reel services

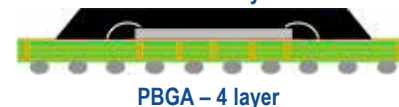



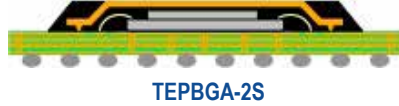
Shipping

- JEDEC outline CO-029 low profile tray

Cross-section PBGA



PBGA Standard Package Offering

| | |
|--|--|
|  <p>PBGA - 2 layer</p> | <p>PBGA (Qualified L2AA/260°C) 2/4/6 Layer 4-Layer with 1 oz (35 µm) Internal Cu Planes Single or Multi-Die</p> |
|  <p>PBGA - 4 layer</p> | |
|  <p>TEPBGA-1</p> | <p>TEPBGA-1 (Qualified L2AA/260°C) 4-Layer with 2 oz (70 µm) Internal Cu Planes Single or Multi-Die</p> |
|  <p>TEPBGA-2</p> | <p>TEPBGA-2 (Qualified L3/260°C) 4-Layer with 2 oz (70 µm) Internal Cu Planes Embedded Cu Heat Spreader (Grounded Option)</p> |
|  <p>TEPBGA-3</p> | <p>TEPBGA-3 (Qualified L3/260°C) 4-Layer with 2 oz (70 µm) Internal Cu Planes Embedded Cu Heat Spreader (Grounded Option) Thermally Enhanced Mold Compound</p> |
|  <p>TEPBGA-2S</p> | <p>TEPBGA-2S (Qualified L3/245°C) 4-Layer with 2 oz (70 µm) Internal Cu Planes Embedded Cu Heat Spreader (Grounded Option) Thermally Enhanced Mold Compound Dummy Si spacer</p> |

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DS520Q
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